UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,663	07/26/2000	Robert L. Bortolotto	CER1023-00	6299

26541 7590 01/21/2004

RITTER, LANG & KAPLAN
12930 SARATOGA AE. SUITE D1
SARATOGA, CA 95070

EXAMINER	
DO, NHAT Q	

ART UNIT	PAPER NUMBER
2663	7

DATE MAILED: 01/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/625,663	BORTOLOTTO ET AL.	
	Examiner	Art Unit	
	Nhat Do	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40 and 42-53* is/are rejected.

7)☒ Claim(s) *41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Status of claims

There are 2 independent claims 43. Accordance with 37 CFR 1.75, which requires the claims shall be numbered consecutively in Arabic numerals. Accordingly, claims 43, 43-52 have been renumbered 43-53 respectively.

Applicant is requested to make appropriate correction to the numbering of the claims and their respective dependencies in respond to this office action.

Claim Objections

1. Claims 34, and 35 objected to because of the following informalities:

The phrase "the method of claim 32" in lines 1 of claims 34, and 35 should be changed to 'the computer program of claim 32' for corresponding.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 7, 9, 10, 19, 20-25, 29-34, 36-38, 44-53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,580,720 to Francis et al.

References appear in parenthesis.

Regarding to claim 1, Francis et al disclose a system comprising:

A plurality of interface cards (I/O ports) for transmitting and receiving data streams (transferring signal between selected I/O ports (Col. 40, lines 39-47));

A cross-connect unit (the switching fabric and the controller constitute a cross connect unit) for routing the data streams received from a first set of said plurality of interface cards to a second set of said plurality of interface cards (the switching fabric delivers signals between I/O ports (Col. 39, lines 1-12; col. 40, lines 40-47)), said cross-connect unit routing each data stream based on an associated matrix (the switching fabric uses one of possible signal paths determined by a controller, wherein a path is identified by I/O ports coupled to corresponding sending and receiving devices (Col. 40, lines 40-60). The examiner is in the position the information about all possible paths is the associated matrix), wherein the associated matrix identifies the interface cards that will receive the data stream (since Francis et al disclose: the path is selected from selected I/O ports (Col. 40, lines 40-45), the examiner is in the position the controller identifies the matrix (path information) by identifying the interface cards (I/O ports)) and an order that the interface cards will receive the data stream (selecting the lowest latency signaling path. If it is not available, selecting the next lowest latency path (Col. 39, lines 1-12; col. 40, lines 54-60). In other words, when the lowest latency path is selected the I/O port of that path is used; when the next lowest latency path is selected another I/O port is used. Therefore, the matrix (path information) identifies and the order of interface cards (I/O ports) that will receive data).

A control unit for controlling the operation of the apparatus (the path selection is controlled by a controller (Col. 40, lines 54-60); and

A back-plane forming connections between the cross-connect unit and each of the plurality of interface cards (I/O ports (IP Rack 1)) are connected to the switching fabric (Hub Rack 2) by cables (Col. 19, lines 61-65)).

Regarding to claim 2, Francis et al disclose:

The associated matrix includes a source point (I/O port of the sending device) and a destination point (I/O port of the receiving device) for each section (signaling path) of the data circuit, wherein a section is defined as a transmission of the data stream from one interface card to another interface card, the source point corresponds to a transmitting interface card and the destination point corresponds to a receiving interface card (as disclosed in the rejection of claim 1, since the controller identifies the paths in term of the interface cards (I/O ports), it is inherent that the matrix (path information) includes a source point (I/O port of the sending device) and a destination point (I/O port of the receiving device) for each section (signaling path) of the data circuit).

Regarding to claim 3, Francis et al disclose:

The associated matrix further includes a next drop point for each destination point so that said cross-connect unit can route the data stream to the next drop point if the receiving interface card associated with the destination point is inoperable (since Francis et al disclose: selecting the next lowest latency path if the first path is unavailable due to inoperable (Col. 39, lines 1-12; col. 40, lines 54-60), the examiner is

in the position the I/O port of the next lowest latency path is the next drop point. Furthermore, Francis et al disclose the fault is failure of I/O ports (PI rack) (Col. 18, lines 11-21)).

Regarding to claim 4, Francis et al disclose:

In the event that consecutive interface cards are inoperable said cross-connect unit can continually utilize the next drop point in the associated matrix to determine the next interface card to receive the data stream (selecting the next lowest latency signal path that is presently available (Col. 41, lines 4-7).

Regarding to claim 5, Francis et al disclose:

The associated matrix further includes a previous point for each source point (the sending I/O port is previous point, and the receiving port is the source port).

Regarding to claim 7, Francis et al disclose:

Each of said plurality of interface cards is connected to all other of said plurality of interface cards through said cross connect unit (Since Francis et al disclose: any device can be connected to any other device that uses the same data transfer protocol (Col. 37, lines 43-46), the examiner is in the position all the I/O ports that uses the same data transfer protocol are said plurality of interface cards).

Regarding to claim 9, Francis et al disclose the switching fabric is an add-drop multiplexer. (Since Francis et al disclose the MIPPSS is connected to user equipment or user system or to another similar MIPPSS (hub-to-hub connection) via either electrical or optical cable (Col. 15, line 55-col. 16, line 3), the examiner is in the position the system is an add-drop multiplex in the situation when data is transferred between the

user terminal and the similar MIPPSS, and the cable between the user terminal and the system is electrical while the cable between the system and the next similar MIPPSS is optical).

Regarding to claim 10, Francis et al disclose:

The interface cards include telecommunication cards (since the I/O ports are used to interconnect the switching system to the other switching system or user system (Col. 15, lines 55-67), they are intercommunication cards).

Regarding to claim 19, Francis et al disclose:

The cross connect unit is passive (the device does not analyze the transferred data (Col. 12, lines 45-50)).

Regarding to claim 20, Francis et al disclose:

The cross-connect unit determines when an interface card is inoperable and utilizes the associated matrix to determine where to route the data stream (the MIPPSS selects the next lowest latency path when the first path is inoperable due to component failure (Col. 39, lines 1-12).

Regarding to claim 21, further to the rejection of claim 1, since Francis et al disclose the system is implemented by software, it is inherent there is memory for storing the path information.

Regarding to claim 22, the claim recites the limitations similar to the rejected limitations of claim 1; therefore claim 22 is also rejected with the same rationale disclosed above.

Regarding to claims 23, 29, the claims recite the limitations similar to the rejected limitations of claim 1; therefore claims 23, and 29 are rejected with the same rationale disclosed above.

Regarding to claim 24, the claim recites the limitations similar to the rejected limitations of claim 4; therefore claim 24 is rejected with the same rationale disclosed above.

Regarding to claim 25, Francis et al disclose:

The matrix that includes a destination point (the I/O port of the first path), a next destination point (the I/O port of the next lowest latency path), and a previous point for each interface card (the I/O port of the sending device).

Regarding to claims 30, and 52, Francis et al disclose:

Means for generating a matrix (available path) that identifies interface cards to receive the data stream, the matrix including destination points and next destination points for each interface card (the controller determines all available paths, which are established between selected I/O ports (Col. 40, lines 40-60));

Means for receiving the data stream at the first interface card (the I/O port coupled to the receiving device);

Means for transmitting the data stream from the first interface card to a cross-connect unit (the I/O port coupled to the sending device);

Means for determining from the matrix that the cross-connect unit should route the data stream to the second interface card (the switching fabric selects the lowest latency path);

Means for determining that the second interface card is inoperable (the controller determines all presently available paths);

Means for determining from the matrix that the cross-connect unit should route the data stream to the third interface card (If the first path is unavailable, selecting the next lowest latency path (Col. 39, lines 1-12; col. 40, lines 40-54)); and

Means for transmitting the data stream from the cross connect unit to the third interface card (selecting the next lowest latency path (Col. 39, lines 1-12; col. 40, lines 40-54)).

Regarding to claims 31, 38, and 53, Francis et al disclose:

The first, the second and the third interface cards are located within a network element (the devices are in a multi-interface switching system (fig. 15A)).

Regarding to claims 32, 33, and 34, further to the rejection of claims 23 24, and 5 respectively, since Francis et al disclose using software to control the system (Col. 11, lines 44-51)), it is inherent that there exist code segments to control the steps of claims 23, and 24.

Regarding to claim 36, further to the rejection of claim 1, the I/O port of the next lowest latency path is considered the next destination point.

Regarding to claims 37, and 38, further to the rejection of claims 30, and 31, since Francis et al disclose using software to control the system (Col. 11, lines 44-51)), it is inherent that there exist code segments to control the steps of claims 37, and 38.

Regarding to claim 46, further to the rejection of claim 23, since Francis et al disclose using software to control the system (Col. 11, lines 44-51)), it is inherent that there exist code segments to control the steps of claim 23.

Regarding to claim 47, Francis et al disclose:

Means for defining the data circuit as a plurality of interface cards that will receive a particular data stream (a controller determines all presently available paths (Col. 40, lines 54-60));

Means for generating a matrix based on the data circuit, the matrix including a destination point and a next destination point for each interface card (the controller determines the latency for all available paths (Col. 40, lines 55-60)); and

Means for routing the data stream to the appropriate interface cards, wherein the data stream is routed to the destination point identified in the matrix, and if the interface card associated with the destination point is inoperable the data stream is routed to the next destination point identified in the matrix (the switching fabric selects the lowest latency path. If the first path is unavailable, selecting the next lowest latency path (Col. 39, lines 1-12; col. 40, lines 40-54)).

Regarding to claim 48, the claim recites the limitation similar to the rejected limitation of claim 4; therefore the claim is also rejected with the same rationale disclosed above.

Regarding to claim 49, the sending I/O port is the previous point.

Regarding to claim 51, the claim recites the limitations similar to the rejected limitations of 46; therefore, the claim 50 is also rejected with the same rationale disclosed above.

Regarding to claim 44, Francis et al disclose:

Connecting a plurality of interface cards to each other through a cross-connect, wherein the manner in which the interface cards are connected defines a data circuit (Connecting I/O ports coupled to the sending devices to the I/O ports coupled the receiving devices (Col. 40, line s40-50));

Establishing a mapping table for the data circuit (determining all possible paths (Col. 54-60), the mapping table including direct connections (the paths includes the lowest latency path) for each interface card (sending I/O port) and next connections (next lowest latency paths) for each interface card (sending I/O Port) (Col. 39, lines 1-12; col. 40, lines 55-60);

Determining that a first interface card (receiving I/O port of the next lowest latency path) that is connected to a second interface card (sending I/O port) and a third interface card is inoperable (the receiving I/O port of the lowest latency path that is not selected)

Connecting the second interface card (the sending I/O port) to the third interface card (the receiving I/O port of next lowest latency path), when the mapping table defines the third interface card as the next connection for the second interface card (the path information indicates next lowest latency path is the second choice).

Regarding to claim 45, further to the rejection of claim 53, since Francis et al disclose using software to control the system (Col. 11, lines 44-51)), it is inherent that there exist code segments to control the steps of claims 44.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6, 8, 11-18, 27-29, 39, 40, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Francis et al.

Regarding to claims 6, 26, 35, and 50, further to the rejection of claims 5, 25, 34, and 46, Francis et al fail to disclose explicitly using the previous point (the I/O port of the first path) when the interface card becomes operational. However it would have been obvious to a person having ordinary skill in the art by the time the invention was made to modify the switching fabric of Francis et al by making it uses the previous point (the I/O interface of the first path) when the interface card (I/O port) become operational. A skilled artisan would have been motivated to do so because the first path is the optimum path (lowest latency path) in the system.

Regarding to claims 8, and 39, further to the rejection of claim 3, Francis et al fail to disclose explicitly the interfaces (I/O ports) are Ethernet interfaces. However, Francis et al disclose the system can be used for any data transfer protocol (Col. 15, lines 37-40). Therefore, it would have been obvious to a person having ordinary skill in the art

by the time the invention was made to make the interfaces (I/O ports) as the Ethernet interfaces (Ethernet I/O ports) when the user system in figure 15A uses Ethernet protocol.

Regarding to claims 11-18, 27, 28, 42, similarly, it would also have been obvious to a person of ordinary skill in the art by the invention was made to make the interfaces (I/O ports) as WDM, TDM, SONET, SDH, PDH, token ring or FDDI interfaces depending on the need.

Regarding to claim 40, Francis et al disclose:

Defining a circuit mapping table which includes information relating to how said interface cards are connected together through the cross-connect (determining the latency of all the presently available paths (Col. 40, lines 54-57); the latency is used for connecting selected I/O ports together (Col. 39, lines 1-12; col. 40, lines 39-50)).

Connecting the remaining interface cards together through the cross-connect, the connections between the remaining interface cards based on information contained in the circuit table (using the latency information to connect selected I/O ports together (Col. 39, lines 1-12; col. 40, lines 39-50)).

Francis et al fail to disclose explicitly detecting when one or more of said interface cards is disconnected from the cross-connect.

However, Francis et al disclose monitoring the status of the interface (Col. 18, lines 1-10). Francis et al also disclose physical components are often remove for maintenance or repair (Col. 5, lines 10-15).

Therefore, it would have been obvious to a person having ordinary skill in the art by the time the invention was made to modify the system of Francis ell al so that it also monitor the when the interface card is disconnected in order to exclude the remove interface from the present available paths.

Regarding to claim 43, further to the rejection of claim 40, since Francis et al disclose using software to control the system (Col. 11, lines 44-51)), it is inherent that there exist code segments to control the steps of claim 40.

Allowable Subject Matter

6. Claim 41 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhat Do whose telephone number is (703) 305-5743. The examiner can normally be reached on 9:00 AM - 6:00 PM (Monday-Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (703) 308-5340. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 872-9306.

Nhat Do
Examiner
Art Unit 2663

ND
January 12, 2004

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 1/12/04